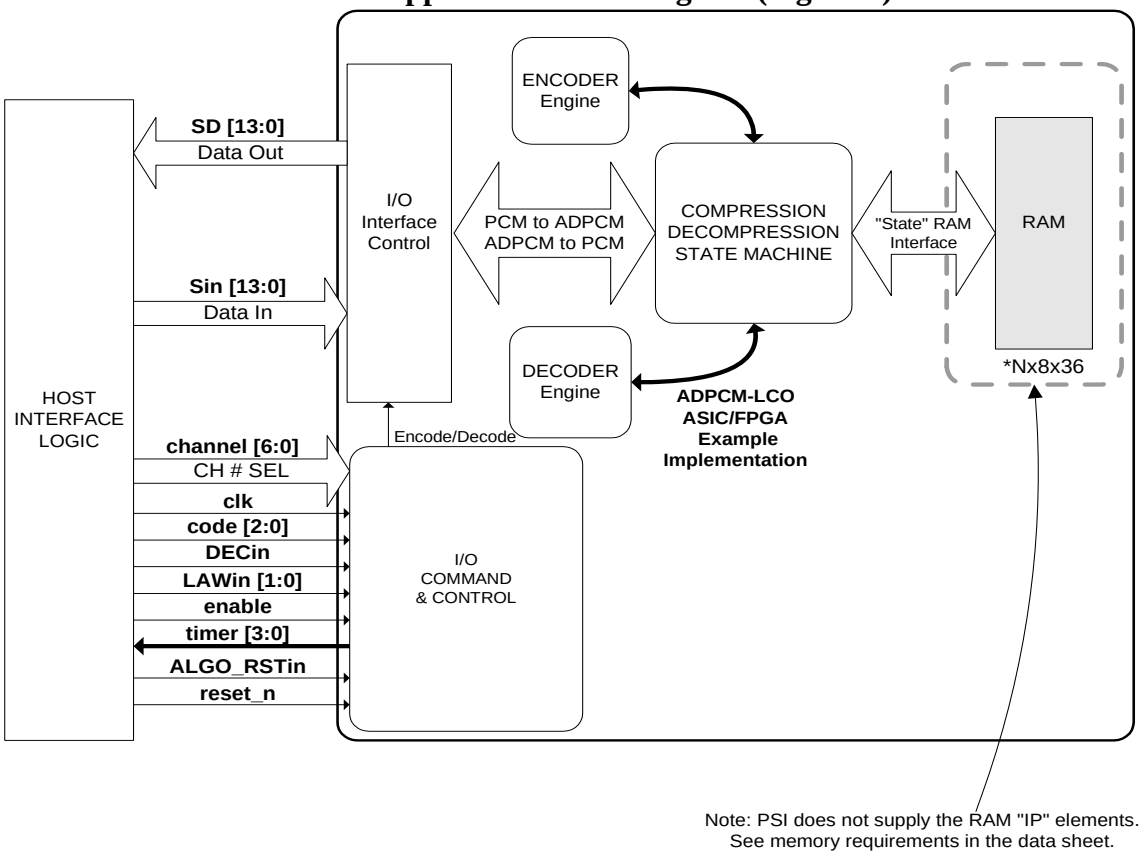
ADPCM-LCO Voice Compression Logic Core

Functional Description

The ADPCM-LCO "logic core" [Adaptive Differential Pulse Code Modulation-**L**ow **C**hannel count **O**ptimized] is a peripheral for digital voice compression/de-compression at 16, 24, 32, 40Kbs rates, as defined in the ITU-T G.726, and G.727 specification. A simple synchronous parallel interface provides (encode "**and**" decode) of 1 to 64 "**full-duplex**" voice channels, or (encode "**or**" decode) of 1 to 128 "**half-duplex**" voice channels. The ADPCM-LCO is designed for "easy" implementation an ASIC, FPGA or element in a SOC design.

Core application block diagram (Figure 1)



ADPCM General Information

ADPCM digital voice encoding and decoding provides a telephone network "toll" quality voice stream. Encoding, via compression techniques allows a reduction of the amount of bandwidth required to transport or store the digital voice samples. Decoding allows the samples to be de-compressed to result in voice, which sounds intelligible and quite normal to the listener. The rate of compression/encoding is relative to the amount of bandwidth saved and also is reflected in sound content of the voice stream. Details of the ADPCM algorithm can be found in the following specifications: ITU-T G.726 and ITU-T G.727.

ADPCM-LCO Core Interface Operation

A synchronous parallel interface to the core provides separate "data" input and output ports. This interface serves as encode (PCM to ADPCM) and decode (ADPCM to PCM) interface for digital voice samples to/from the host system processor. Configuration of this interface is required prior to the setup of the valid data to be processed (Channel #, Code rate, Law type, encode or decode request signals). The configuration signal inputs to the core are specific to a given channel #. Use of the parallel data interface provides the user with dedicated encode and decode ports for voice processing functions (respectively compression and decompression of voice traffic).

Note: Reference "**ITU-T G.711**" specifications, for PCM Pulse Code Modulation information and descriptions.

ADPCM-LCO Core Interface Definitions (Table 1)

Signal Name	Core Source	Functional Description
Control/Status Interface		
channel [6:0]	Input	Current channel address. 0 to maximum channel count. [6:0]="128" channel selects
clk	Input	System Clock input, clock fans out to all associated rams.
Code [2:0]	Input	Selects the standard type and coding rate of the ADPCM core channel. [0XX]= (G.727 codes), [1XX]= G.726 codes. [X00]= 16Kbs, [X01]= 24Kbs, [X10]= 32Kbs, [X11]= 40Kbs
DECin	Input	Channel-by-channel selection of encode or decode function. Logic low = ADPCM Encode. Logic high = ADPCM Decode.
LAWin [1:0]	Input	A-law μ-law select. Channel by channel selection of encoding law. [00]= Linear, [01]=μ-law. [10]= A-law (with even bit inversion), [11]= A-law (with-out even bit inversion).
reset_n	Input	Core hardware Reset. Active low.
timer [3:0]	Output	Synchronous core timer outputs, see timing diagrams.
ALGO_RSTin	Input	ADPCM algorithm reset, as defined in the ITU G.726. Active high.
Enable	Input	Core input valid strobe. Active high. High going edge indicates valid inputs on Enc_dec, Law, S, Chnl and Code.
Input Interface		
Sin [13:0]	Input	"Data byte in interface". Linear [14 bit], μ-Law/A-Law [8bit]. ADPCM for **decode**. PCM for **encode**. PCM data byte represented as [MSB ... LSB]. Linear (2's Complement "G.711")=[13:0] μ-Law/A-Law =[7:0] ADPCM 40Kbs [7:3], 32Kbs [7:4], ADPCM 24Kbs [7:5], ADPCM 16Kbs [7:6].
Output Interface		
SD [13:0]	Output	"Data byte out interface". Linear [14 bit], μ-Law/A-Law [8bit]. PCM for **decode**. ADPCM for **encode**. PCM data byte represented as [MSB ... LSB]. Linear (2's Complement "G.711")=[13:0] μ-Law/A-Law =[7:0] ADPCM 40Kbs [7:3], 32Kbs [7:4], ADPCM 24Kbs [7:5], ADPCM 16Kbs [7:6].

Core Reset and Initialization

Hardware reset of the core is accomplished by the assertion (active low) of the “reset_n” input.

The “ALGO_RSTin” signal (active high) is specific to the testing and verification of the ADPCM encoder/decoder core section to force all internal memory devices, registers, and state machines of an associated channel to a known state. This operation requires each channel used to be reset independently; “ALGO_RSTin” must be high for a minimum of sixteen clock cycles for each channel address. Usage of this signal is primarily for ITU vector testing of the core, the signal should be asserted along with the first vector of some ITU files. Specific information on testing of the core will be made available to users of the core.

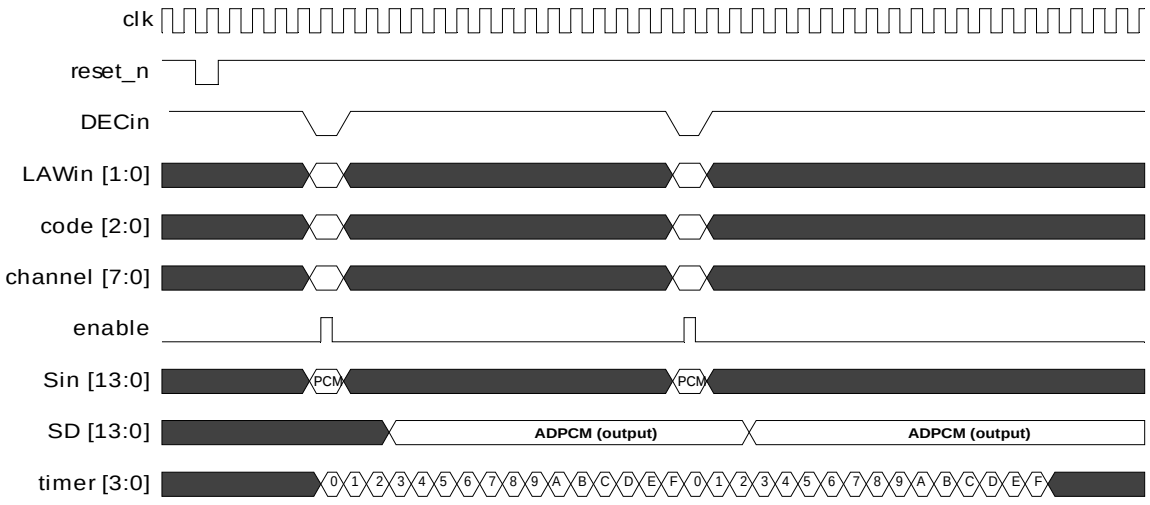
Clock

The “clk” input requires a minimum value of: the required (half-duplex) channels multiplied by sampling rate (8000) “8Khz” multiplied by 16 (“clk” cycles required to function at full rate voice). For example a 128 (half-duplex) channel core configuration would require a minimum input clock of “16.384” MHz (128 x 8000 x 16).

Encode Operation

Data (un-compressed voice sample “PCM”) is presented to the input interface Sin [13:0] with the desired channel #(channel), Code rate (code), Law type (LAWin) and a valid Encode/Decode signal (DECin=0”Encode”). The host will then assert the enable signal (active high) to latch and feed the data to the core. Verification of the completed cycle is indicated by the output value of the timer [3:0] signal. Typically this signal is used to generate an interrupt input serviced by the host as an indication of a “completed encode cycle”. The host processor can now retrieve the compressed (ADPCM) voice sample from the SD [13:0] interface.

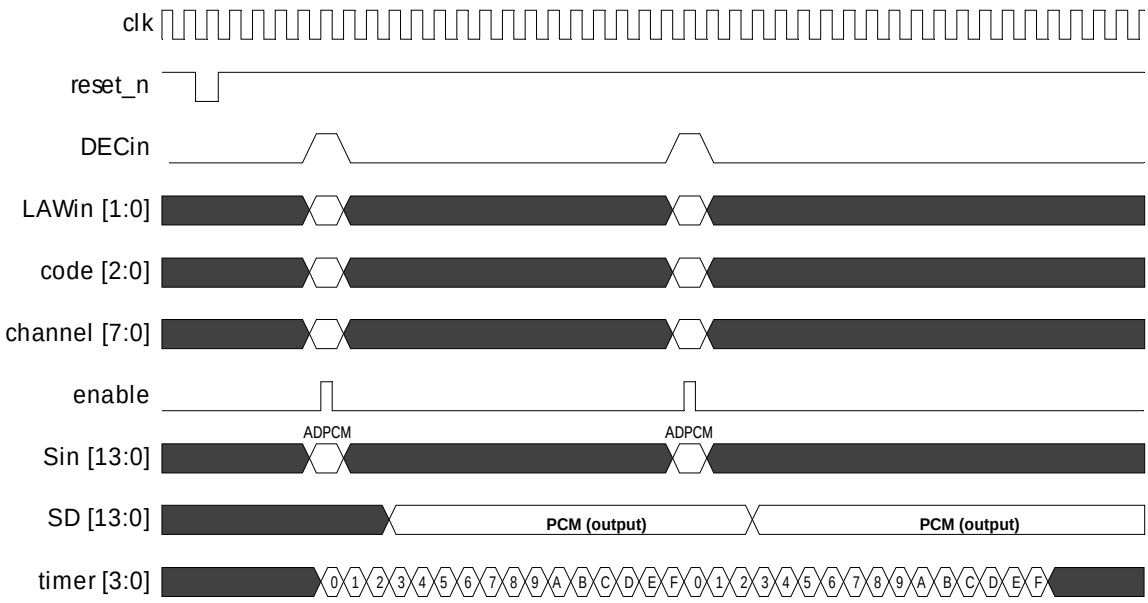
General Encode Timing (Figure 2)



Decode Operation

Data (compressed voice sample" ADPCM) is presented to the input interface Sin [13:0] with the desired channel #(channel), Code rate (code), Law type (LAWin) and a valid Encode/Decode signal (DECin=1 "Decode"). The host will then assert the enable signal (active high) to latch and feed the data to the core. Verification of the completed cycle is indicated by the output of the timer [3:0] signal. Typically this signal is used as an interrupt input serviced by the host as an indication of a "completed decode cycle". The host processor can now retrieve the un-compressed (PCM) voice sample from the SD [13:0] interface.

General Decode Timing (Figure 3)



Encode/Decode Notes:

Back-to-back enable strobes must be at least 16 clock cycles apart. If they are spaced further, the ADPCM-LCO core will "idle" until the 'next' sample is presented.

Timer signal

The four bit timer signal provides a count of the event processing when the core is running compression and decompression operations. The value of the timer indicates specific events from encode and decode process, (idle/ready state timer = [1111] or "F", encode or decode operation cycle complete data is valid timer = [0010] or "2". Use of these signals provides a flexible and universal interface to any system.

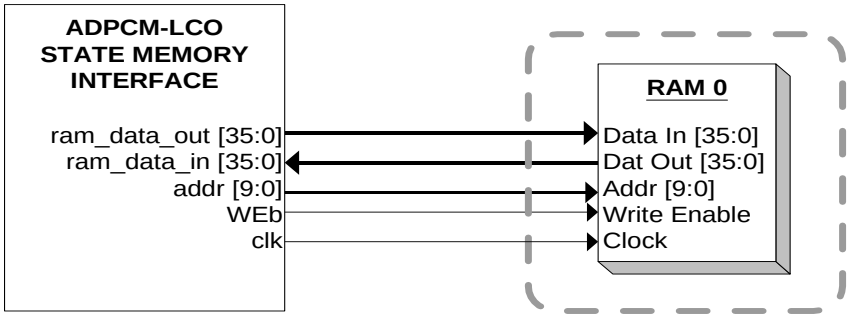
Core Memory Requirements

The core "RAM" requirements are dependent on the number of supported channels. Designs with low channel counts may only require the memory to be implemented as registers. A single synchronous "Nx8x36" bit Static Ram is required for use by each half-duplex channel, where "N" is the number of "supported voice channels" by the core configuration. A single RAM interface consists of a 36 bit wide data in and data out interfaces, 10bit address, write enable, and a synchronous clock interface. The basic timing of the RAM is a single clock (system clock) cycle read and write function.

Note: RAM timing is a function of channel count, and system clock frequency, and typically verified via static timing analysis, or gate level simulations.

Note: adpcm_lco core output Web is an ACTIVE LOW write enable for the ram. Be sure to configure the RAM block for active LOW write enable.

ADPCM-LCO RAM Connection Diagram (Figure 4)



RAM Interface Definitions (Table 1)

Core Signal Name	RAM Interface Signal Source	Functional description
ram_data_in [23:0]	Output	ADPCM RAM write Data pins
ram_data_out [23:0]	Input	ADPCM RAM read data.
addr [9:0]	Output	ADPCM RAM Address pins
Web	Output	ADPCM RAM Write enable. Active low write
Clk	Output	Core clk input

ADPCM-LCO Product Specifications (Table 2)

Bus Interface	Synchronous Parallel
Internal Ram requirements for each "Half-Duplex" Channel	"8x36" bits, Synchronous Bus.
Operating frequency/Channel capacity	@1.024MHz, 128 Channels half duplex 64 Channels full-duplex **50% duty cycle clock required**
Voice standards compliance	ITU-T G.726, (Optional G.727 support by request)
Logic size requirements in gates	Available on request
Die size area	Available on request
ADPCM Code rates	(16, 24, 32, 40) Kbs

ADPCM Code Formats	A-Law, μ-Law, Linear (2's Complement "**G.711**")

Core Implementation

PSI is committed to aiding in the design effort required to employ this core into the targeted design. The advantage of core customization to the user is very attractive in relation to the following benefits:

- The core is scaleable and interface "flexible" for specific applications.
- Cost reduction (by increased density), reduced power consumption, board space "real-estate" reduction, power supply requirements.
- Specific interface design may reduce the over-all function processing and hardware/software system resource requirements.
- Standards based and verified voice-processing functions.
- Simple design implementation as a FPGA, ASIC or SOC element.
- Reference "Demo" platform available for prototyping and core verification.

ADPCM-LCO Deliverables:

PSI has specified the following as a basic set of product deliverables.

- A specification of the "RAM timing" to be provided for the core requirements.
- A test bench for the core, and control scripts to run Verilog simulations that exercise all ITU standard vectors for the G.726 supported code rates.
- A test bench for the core, and control scripts to run Verilog simulations that exercise all ITU standard vectors for the G.727 supported code rates.
- A synthesis script/shell to assist in synthesis of the core.
- Test bench core coverage analysis document.
- Verilog RTL I.P. Core.
- Technical support.

Options for the ADPCM-LCO core include:

The following items are available by request as additional options for the core.

- Scalable encoding/decoding channel count.
- Auto-channel mode.
- Ram Test.
- Custom Bus Interface options.
- FPGA specific targeting.
- VHDL Testbench for use with VHDL gate level netlist.
- Asynchronous bus interface.

License Information

PSI is committed to offering a range of agreements to satisfy all parties involved. We are committed to making your project a success by providing flexible license terms and conditions.

PSI Reference Documents

Check our website for latest information:

- Application notes.
- Demo Board Reference Users manual.
- White papers.
- Product briefs.

Sales information

Upon request, PSI shall complete a quotation for this product, including pricing, deliverables list, and licensing agreements.

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