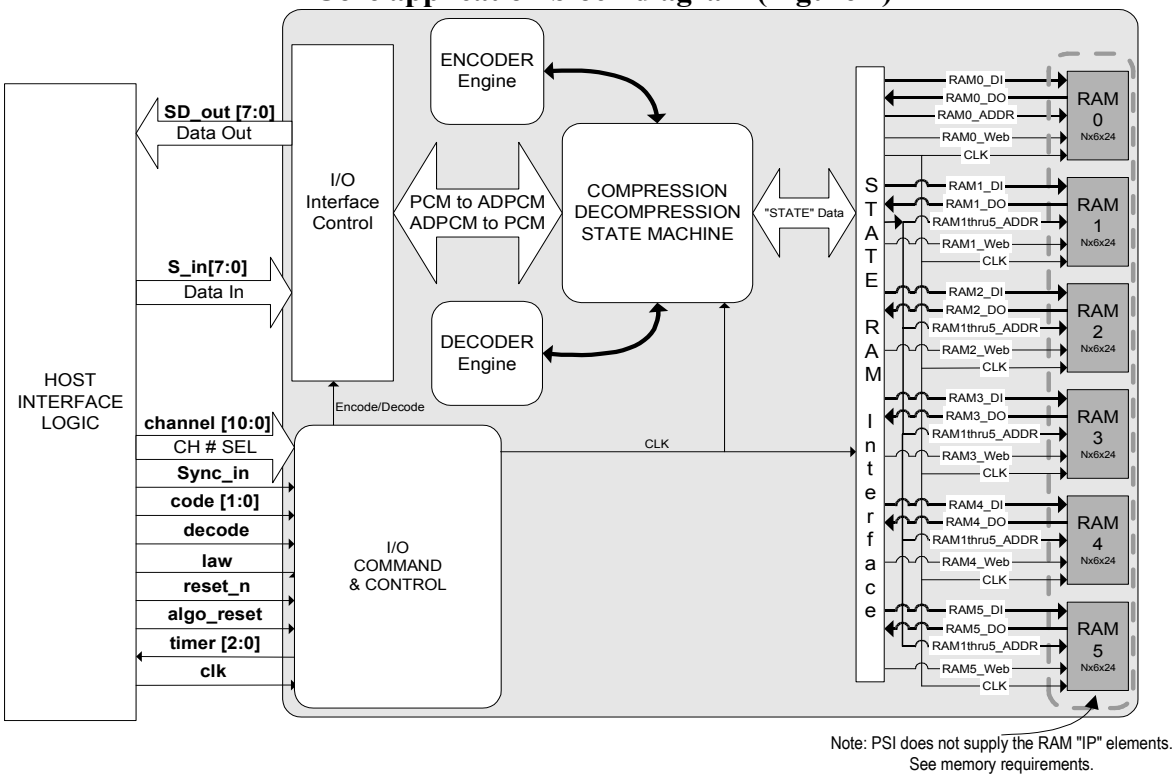
ADPCM-HCO Voice Compression Logic Core

Functional Description

The ADPCM-HCO "logic core" [Adaptive Differential Pulse Code Modulation-**H**igh **C**hannel count **O**ptimized] is a peripheral for digital voice compression (16, 24 and 32Kbs rates) as defined in the ITU-T G.726 specification. A simple synchronous parallel interface provides (encode "**and**" decode) of 1 to 672 "**full-duplex**" voice channels, or (encode "**or**" decode) of 1 to 1344 "**half-duplex**" voice channels. The logic core supports single clock cycle encoding/decoding of a digital voice sample. The ADPCM-HCO is designed for "easy" implementation as an ASIC, FPGA or element in a SOC design.

Core application block diagram (Figure 1)



Note: PSI does not supply the RAM "IP" elements.
See memory requirements.

ADPCM General Information

ADPCM digital voice encoding and decoding provides a telephone network "toll" quality voice stream. Encoding, via compression techniques, allows a reduction of the amount of bandwidth required to transport or store the digital voice samples. Decoding allows the samples to be de-compressed to result in voice, which sounds intelligible and quite normal to the listener. The rate of compression/encoding is relative to the amount of bandwidth saved and also is reflected in sound content of the voice stream. Details of the ADPCM algorithm can be found in the following specifications: ITU-T G.726.

ADPCM-HCO Core Interface Operation

A synchronous parallel interface to the core provides separate "data" input and output ports. This interface serves as encode (PCM to ADPCM) and decode (ADPCM to PCM) interface for digital voice samples to/from the host system processor. Configuration of this interface is required prior to the setup of the valid data to be processed (Channel #, Code rate, Law type, encode or decode request signals). The configuration signal inputs to the core are specific to a given channel #. Use of the parallel data interface provides the user with dedicated encode and decode ports for voice processing functions (respectively compression and decompression of voice traffic).

Note: Reference "**ITU-T G.711**" specifications, for PCM Pulse Code Modulation information and descriptions.

ADPCM-HCO Core Interface Definitions (Table 1)

Signal Name	Core Source	Functional Description
Control/Status Interface		
channel [10:0]	Input	Current channel address. 0 to maximum channel count. [10:0]= "1344" channel selects
clk	Input	System Clock input, clock fans out to all associated rams.
code [2:0]	Input	Selects the standard type and coding rate of the ADPCM core channel. [0XX]= (Optional unsupported codes), [1XX]= G.726 codes. [X00]= 16Kbs, [X01]= 24Kbs, [X10]= 32Kbs, [X11]= reserved
decode	Input	Channel-by-channel selection of encode or decode function. Logic low [0] = ADPCM Encode. Logic high [1] = ADPCM Decode.
law [1:0]	Input	A-law μ-law select. Channel by channel selection of encoding law. [00]= Linear, [01]=μ-law. [10]= A-law w/o even bit inversion, [11]= A-law with even bit inversion.
reset_n	Input	Core hardware Reset. Active low.
timer [2:0]	Output	Synchronous core timer outputs, see timing diagrams.
algo_reset	Input	ADPCM algorithm reset, as defined in the ITU G.726. Active high.
enable	Input	Inputs valid strobe. Active high. High going edge indicates valid inputs on Enc_decb, Law, Chnl, Code and S [13:0] "data Inputs".
Input Data Interface		
S_in [13:0]	Input	"Data byte in interface". Linear [14 bit], μ-Law/A-Law [8bit]. "ADPCM" for **decode**. "PCM" for **encode**. PCM data byte represented as [MSB ... LSB]. Linear (sign and magnitude)=[13:0] μ-Law/A-Law =[13:6] ADPCM 32Kbs [13:10], ADPCM 24Kbs [13:11], ADPCM 16Kbs [13:12].
Output Data Interface		
SD_out [13:0]	Output	"Data byte out interface". Linear [14 bit], μ-Law/A-Law [8bit]. "PCM" for **decode**. "ADPCM" for **encode**. PCM data byte represented as [MSB ... LSB]. Linear (sign and magnitude)=[13:0] μ-Law/A-Law =[13:6] ADPCM 32Kbs [13:10], ADPCM 24Kbs [13:11], ADPCM 16Kbs [13:12].

Core Reset and Initialization

Hardware Reset of the core is accomplished by the assertion (active low) of the "reset_n" input.

The "algo_reset" signal (active high) is specific to the ADPCM encoder/decoder core section to force all internal memory devices, registers, and state machines of a associated channel to a known state. This operation requires each channel used to be "reset" independently; algo_reset must be high for a minimum of sixteen clock cycles for each channel address. Usage of this signal is primarily for ITU vector testing of the core.

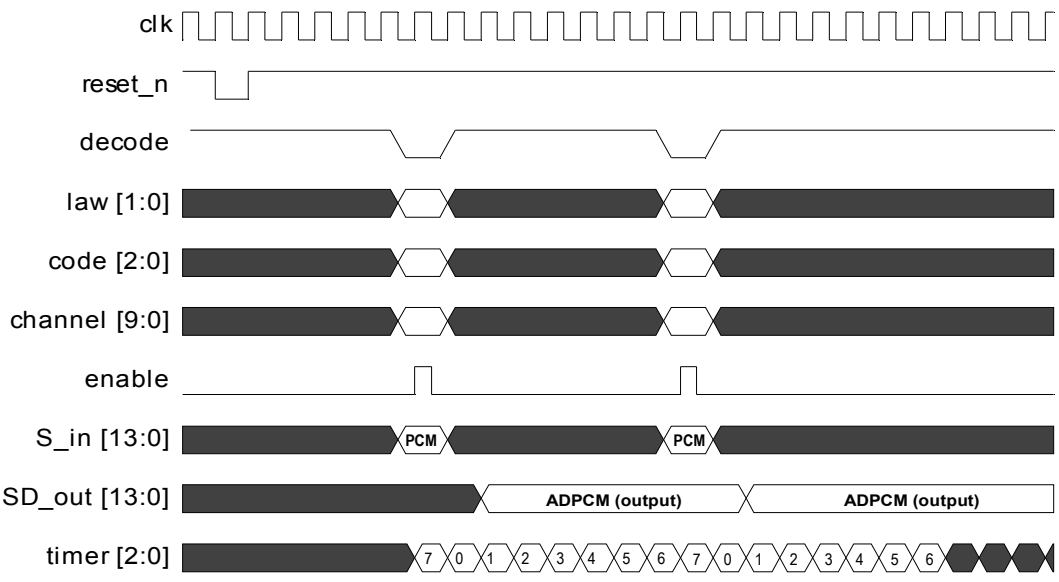
Clock

The "clk" input requires a minimum value of: the required (half-duplex) channels multiplied by sampling rate (8000) "8Khz" multiplied by 8 ("clk" cycles required to function at full rate voice). For example a 672 (half-duplex) channel core configuration would require a minimum input clock of "43.008" MHz (672 x 8000 x 8).

Encode Operation

Data (un-compressed voice sample "PCM") is presented to the input interface S_in [13:0] with the desired channel #(channel), Code rate (code), Law type (law) and a valid Encode/Decode signal (decode=1"Encode"). The host will then assert the "enable" signal (active high) to latch and feed the data to the core. Verification of the completed cycle is indicated by the output of the timer [2:0] signal. Typically this signal is used as an interrupt input serviced by the host as an indication of a "completed encode cycle". The host processor can now retrieve the compressed (ADPCM) voice sample from the SD_out [13:0] interface.

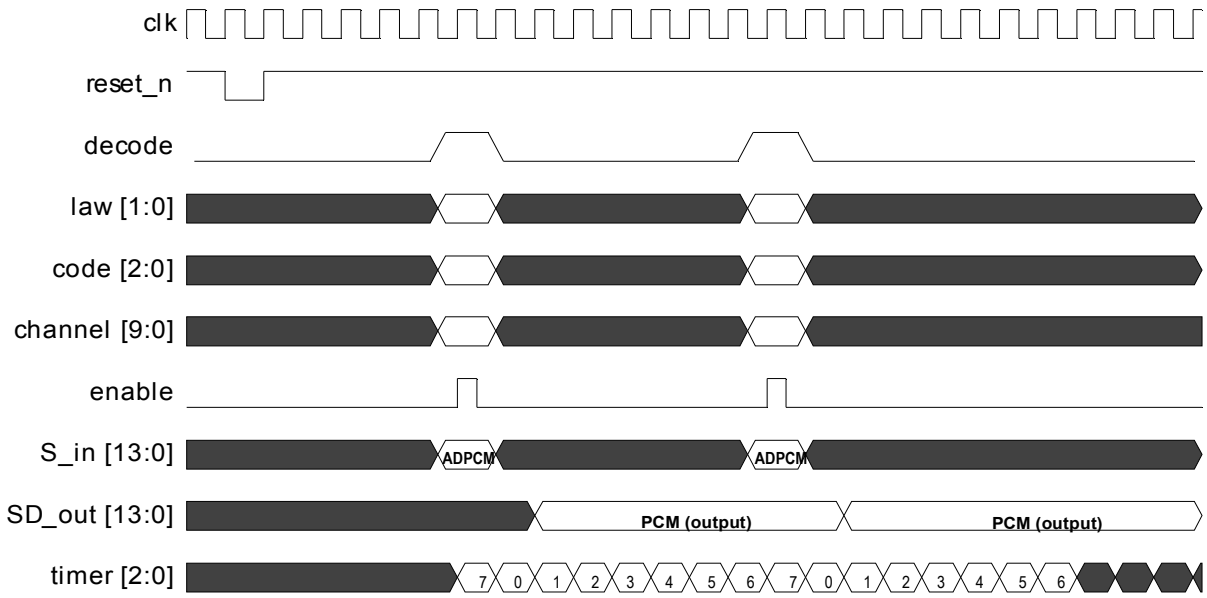
General Encode Timing (Figure 2)



Decode Operation

Data (compressed voice sample" ADPCM) is presented to the input interface S_in [13:0] with the desired channel #(channel), Code rate (code), Law type (law) and a valid Encode/Decode signal (Enc_decb=1 "Decode"). The host will then assert the enable signal (active high) to latch and feed the data to the core. Verification of the completed cycle is indicated by the output of the timer [2:0] signal. Typically this signal is used as an interrupt input serviced by the host as an indication of a "completed decode cycle". The host processor can now retrieve the un-compressed (PCM) voice sample from the SD_out [13:0] interface.

General Decode Timing (Figure 3)



Encode/Decode Notes:

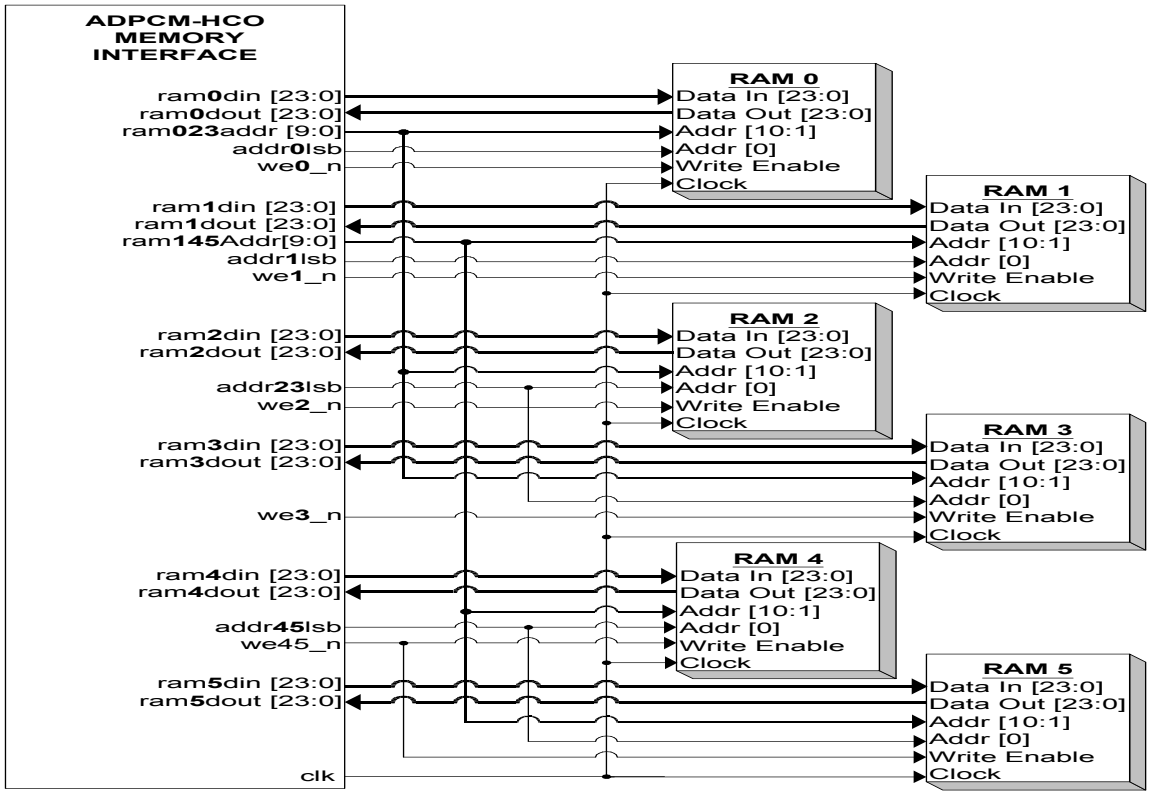
Back-to-back "enable" strobes must be at least 8 clock cycles apart. If they are spaced further, the ADPCM-HCO core will "idle" until the 'next' sample is presented to the data input interface.

Core Memory Requirements

The core "RAM" requirements are dependent on the number of supported channels. Designs with low channel counts may only require the memory to be implemented as registers. Six synchronous "Nx6x24" bit Rams are required for use by each half-duplex channel, where "N" is the number of "supported voice channels" by the core configuration. A single RAM interface consists of a 24bit wide data in and out interfaces, 11bit address, write enable, and a synchronous clock interface.

Note: Ram timing is a function of channel count, and system clock frequency, and typically verified via static timing analysis, or gate level simulations.

ADPCM-HCO RAM Connection Diagram (Figure 4)



RAM Interface Definitions (Table 2)

Signal Name	Ram Interface Signal Source	Functional Description
ram0din [23:0]	Output	RAM0 write data interface
ram0dout [23:0]	Input	RAM0 read data interface
ram023addr [9:0]	Output	MSB address shared by RAM0, RAM2, RAM3.
Addr0lsb	Output	RAM0 LSB Address pin.
we0_n	Output	RAM0 Write enable. Active low write.
ram1din [23:0]	Output	RAM1 write data interface
ram1dout [23:0]	Output	RAM1 write data interface.
ram145addr [9:0]	Output	MSB Address shared by RAM1, RAM4, RAM5.
addr1lsb	Output	RAM1 LSB Address pin.
we1_n	Output	RAM1 Write enable. Active low write.
ram2din [23:0]	Output	RAM2 write data interface.
ram2dout [23:0]	Input	RAM2 read data interface.
addr23lsb	Output	LSB address, shared by RAM2 and RAM3.
we2_n	Output	RAM2 Write enable, active low write.

ram3din [23:0]	Output	RAM3 write data interface.
ram3dout [23:0]	Input	RAM3 read data interface.
we3_n	Output	RAM3 Write enable, active low write.
ram4din [23:0]	Output	RAM4 write data interface.
ram4dout [23:0]	Input	RAM4 read data interface.
addr45lsb		LSB address, shared by RAM4 and RAM5.
we45_n	Output	RAM4 and RAM5 Write enable. Active low write.
ram5din [23:0]	Output	RAM5 write data interface.
ram5dout [23:0]	Input	RAM5 read data interface.
clk	Output	System clock from the core clk input

ADPCM-HCO Product Specifications (Table 3)

Bus Interface	Synchronous Parallel
Internal Ram requirements for each "Half-Duplex" Channel	2X24X6 bits, Synchronous Bus.
Operating frequency/Channel capacity	@43.008MHz, 672 Channels half duplex 336 Channels full-duplex @86.016Mhz, 1344 channels half-duplex 672 channels full-duplex **50% duty cycle required**
Voice standards compliance	ITU-T G.726, (Optional G.727 support by request)
Logic size requirements in gates	Available on request.
Die size area	Available on request.
ADPCM Code rates	(16, 24, 32) Kbs
ADPCM Code Formats	A-Law, μ-Law, 14 bit Linear

Core Implementation

PSI is committed to aiding in the design effort required to employ this core into the targeted design. The advantage of core customization to the user is very attractive in relation to the following benefits:

- The core is scaleable and interface "flexible" for specific applications.
- Cost reduction (by increased density), reduced power consumption, board space "real-estate" reduction, power supply requirements.
- Specific interface design may reduce the over-all function processing and hardware/software system resource requirements.
- Standards based and verified voice-processing functions.
- Simple design implementation as a FPGA, ASIC or Soc element.

ADPCM-HCO Deliverables:

PSI has specified the following as a basic set of product deliverables.

- A specification of the "RAM timing" to be provided for the core requirements.
- A test bench for the core, and control scripts to run Verilog simulations that exercise all ITU standard vectors for the G.726 supported rates.
- A synthesis script/shell to assist in synthesis of the core.
- Test bench core coverage analysis document.
- Verilog RTL I.P. Core.
- Technical support.

Options for the ADPCM-HCO core include:

The following items are available by request as additional options for the core.

- Scalable encoding/decoding channel count.
- Auto-channel mode.
- Ram Test.
- Logic BIST.
- Custom Bus Interface options.
- FPGA specific targeting.
- VHDL code format (future releases).
- Asynchronous bus interface.
- ITU-T G.727 support.

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PSI Reference Documents

Check our website for latest information:

- Application notes.
- White papers.
- Product briefs.

Sales information

Upon request, PSI shall complete a quotation for this product, including pricing, deliverables list, and licensing agreements.

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